SPECIFICATIONS

PXIe-1487

PXI FlexRIO GMSL Interface Module

This document lists the specifications for the following variants of the PXIe-1487:

- PXIe-1487 FlexRIO GMSL2 Deserializer
- PXIe-1487 FlexRIO GMSL2 Serializer
- PXIe-1487 FlexRIO GMSL2 SerDes

Note If you purchased the PXIe-1487 as part of an NI system, refer to your system documentation for application-specific specifications.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ±5 °C
- Installed in chassis with slot cooling capacity ≥58 W[1]

[1] The PXIe-1487 SerDes module can operate in a chassis with a slot cooling capacity of <58 W in a restricted user mode.

Serial Device Compatibility

Refer to the following information to verify that the PXIe-1487 module chip set is compatible with your serial device or camera.

Chip set brand	Maxim Integrated
Module deserializer	MAX9296A
Module serializer	MAX9295A

Note Contact the manufacturer of your serial device or camera for details on compatibility with the PXIe-1487 module.

Note The PXIe-1487 does not support GMSL1 chip sets.

Bus Interface

Form factor	PCI Express Gen-3 x8

Reconfigurable FPGA

The following table lists the specifications for the PXIe-1487 FPGA.

FPGA	KU11P
LUTs	298,560
DSP48 slices (25 × 18 multiplier)	2,928
Embedded Block RAM	21 Mb
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)
Data transfers	DMA, interrupts, programmed I/O
Embedded UltraRAM™	22 Mb
Number of DMA channels	60

Note These values reflect the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Serial I/O Characteristics

Input Channels

Connector label	SI
Connector type	FAKRA Male Code Z, coaxial
PoC output range, AUX power maximum	9 V to 30 V, 800 mA per channel
PoC output range, internal power supply	
Nominal voltage	12 V
Maximum current	400 mA per channel, 2 A total
I/O standard	GMSL2 with power over coax (PoC)
Maximum data rate	6 Gb/s

Output Channels

Connector label	SO
Connector type	FAKRA Male Code Z, coaxial
PoC input range	
Nominal voltage	9 V to 30 V
Maximum current	800 mA per channel
I/O standard	GMSL2 with power over coax (PoC)
Maximum data rate	6 Gb/s

AUX Power Channels

Power sink or source maximum voltage	9 V to 30 V
Power sink or source maximum current	800 mA per channel
Power connector type	Conn Terminal Block, Weidmuller part number 2439690000

Power connector wiring	
Gauge	0.08 mm^2 to 0.5 mm^2 (28 AWG to 20 AWG)
Wire strip length	8 mm
Terminal connection type	Tension clamp
Retention	External strain relief of AUX power connections recommended

PXIe-1487 Deserializer

Input channels	8
Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2
CSI-2 interface	4 lane, 1200 Mbps per lane, no lane swaps or inversions

PXIe-1487 Serializer

Output channels	8
Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2
CSI-2 interface	4 lane, 1200 Mbps per lane, no lane swaps or inversions

PXIe-1487 SerDes

Input channels	4
Output channels	4
Maximum Tap pairs per module	4
Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2
CSI-2 interface	4 lane, 1200 Mbps per lane, no lane swaps or inversions

Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

Note Do not position product so that it is difficult to disconnect power.

Note If you are powering the PXIe-1487 using your PXIe chassis backplane, refer to the chassis specifications for detailed information about your internal power supply.

Backplane Power Source

Table 1. Backplane Power

Voltage (V)	Maximum Current (A)
3.3	3.0
12	6.0

Total power	82 W, maximum

Power over Coax (PoC) Source

External power supply	
Voltage range	9 V to 30 V
Maximum current	800 mA per channel, up to 8 channels
Internal power supply	
Nominal voltage	12 V
Maximum current	400 mA per channel, up to 2 A total
Diagnostic PoC measurement	
Current measurement range	50 mA to 800 mA
Current measurement accuracy	
50 mA to 100 mA	±20%
100 mA to 800 mA	±15%
Voltage measurement range	9 V to 30 V
Voltage measurement accuracy[2]	±5%

[2] Due to resistive (IR drop) losses in the circuit, actual voltage measurement accuracy depends on the load of the PoC circuit.

Environmental Characteristics

Temperature	
Operating	0 °C to 55 °C[3]
Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

Physical

Dimensions	3U, two-slot PXI Express module, 21.6 cm × 4.1 cm × 13.0 cm (8.5 in. × 1.6 in. × 5.1 in.)
Weight	692 g (24.38 oz)

Timing and Synchronization

Timebase	100 MHz, shared by all ports, disciplined by PXI_Clk100
Trigger I/O source	PXI_Trig <0:7>

[3] The PXIe-1487 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the *PXI Chassis Manual* for specifications to determine the ambient temperature ranges your chassis can achieve.

PXIe-1487 Front Panels

Figure 1. PXIe-1487 Deserializer Front Panel

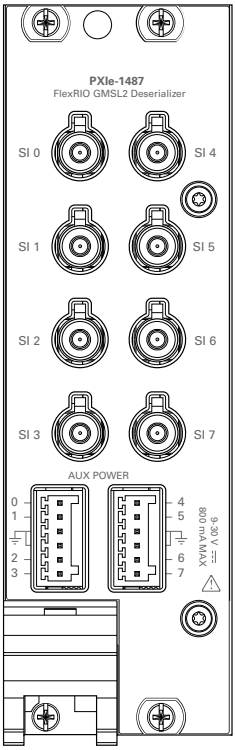


Figure 2. PXIe-1487 Serializer Front Panel

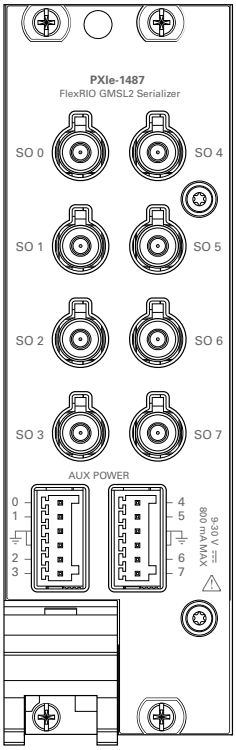
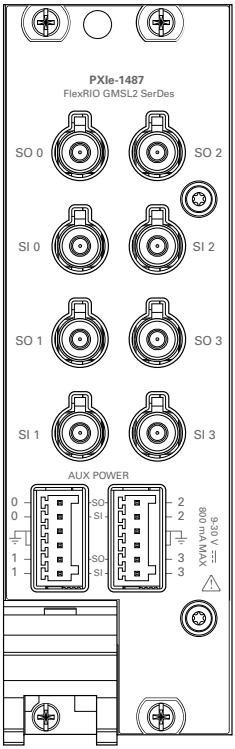


Figure 3. PXIe-1487 SerDes Front Panel



378339A-02 January 6, 2021